

Comparative Evaluation of Generalized Multicell Impedance Source Inverter for Drives

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ABSTRACT

Voltage-Source Inverter is limited by its only voltage step-down operation. In adding with extra boosting the flexibility is kept active for the number of semiconductors which is unchanged, voltage-type Z-source inverter was earlier proposed. This new class of inverter is generally less sensitive to electromagnetic noises. However, their boosting capabilities are anyhow less with high component stresses and poorer spectral performances caused by low modulation index ratios. Their boosting gains are, therefore, restricted in practice. To overcome these we use the generalized switched-inductor Z-source inverter is proposed, By comparing with PWM technique and SPWM technique, whose extra boosting abilities and other advantages have been verified in simulation analysis and experiment.

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1. INTRODUCTION

Modern electrical systems like distributed generators, power conditioners, and industrial drives have raised the importance of dc-ac inverters, through which energy is appropriately conditioned. Although well established now, existing popular inverter topologies still have some constraints to resolve with the first being their inflexible voltage or current conversion ranges. To be more precise, existing voltage-source inverter (VSI) can only perform voltage step-down operation. Voltage and current step-up flexibility can surely be added by connecting appropriate dc-dc converters to the traditional inverters, which probably would be the most commercially viable approach because of its simplicity. Z source inverter also finds in application in electric vehicles where drive voltage stress and controllability is a major factor [11]. Indeed, research in Z-source inverters has progressed actively with their modulation [2], modelling [3], control [4], [5], component sizing and applications, [7]–[9] now being addressed. Recently, another interest has surfaced, and that is to address the limited practical conversion ranges of the Z-source inverters. The Z source inverters with intelligent control and renewable source for maximum output have also been an area of interest for researchers [10]. Although conversion gains of the Z-source inverters are theoretically infinite, practical issues like higher semiconductor stresses and poorer spectral performances can constrain their highest achievable limits. These constraints are undeniably linked to the trade off between modulation ratios and shoot through duration experienced by the Z-source inverters. Each technique has its own advantages and disadvantages that might better suit certain applications. The final decision on which to select is, therefore, dependent on the problems under consideration, individual judgments, preferences. The belief might have led to the development of various dc-ac inverters found in the literature. Among them, the most noticeable at present might be the voltage Z-source inverter, whose layouts are shown in Figure 1 [1]. characteristics such

as bidirectional energy flow capability, it provides sinusoidal input and output waveform with minimum high order harmonics and no sub harmonics, The special Z-network, comprising two capacitors and two inductors, connected to the well known three phase bridge, as shown in Figure 1, allows working in buck or boost modes using the ST state. The ZSI advantageously utilizes the ST states to boost the dc-link voltage by gating on both the upper and lower switches of a phase leg. In addition, a ST state caused by Electromagnetic Interference (EMI) noise does not destroy the circuit. Therefore a more reliable single stage power converter for both buck and boost power conversion is obtained.

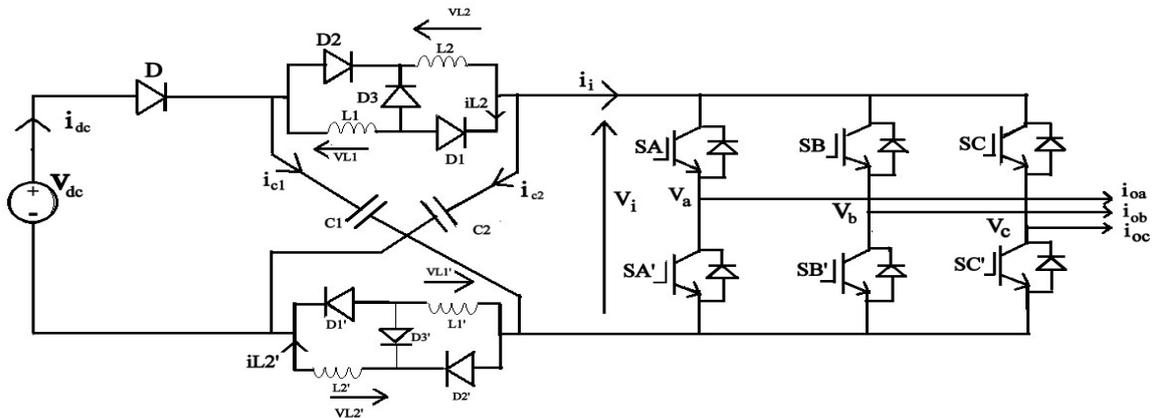


Figure 1. Topology of voltage type SL Z-Source Inverter

2. GENERALIZED MULTICELL SL TOPOLOGY

The SL topology is generalized in Figure 2, where the generic cell identified is shown at the lower right corner. It consists of one inductor L_n and three diodes D_{3n-1} , D_{3n-2} , and D_{3n} for the n th cell. This cell can be duplicated $2N$ times (where N is an integer), divided equally between the upper and lower dc rails, and connected as in Figure 2. Note that inductors L_{2N+1} and L_{2N+2} are not included in the generic cells, but can rather be viewed as the original two inductors found in Figure 1 for the traditional voltage-type Z-source inverter. It thus appears that the style of forming the generic cell allows the generalized SL topology to be viewed as adding extra cells to the original two inductors rather than to replace them [12].

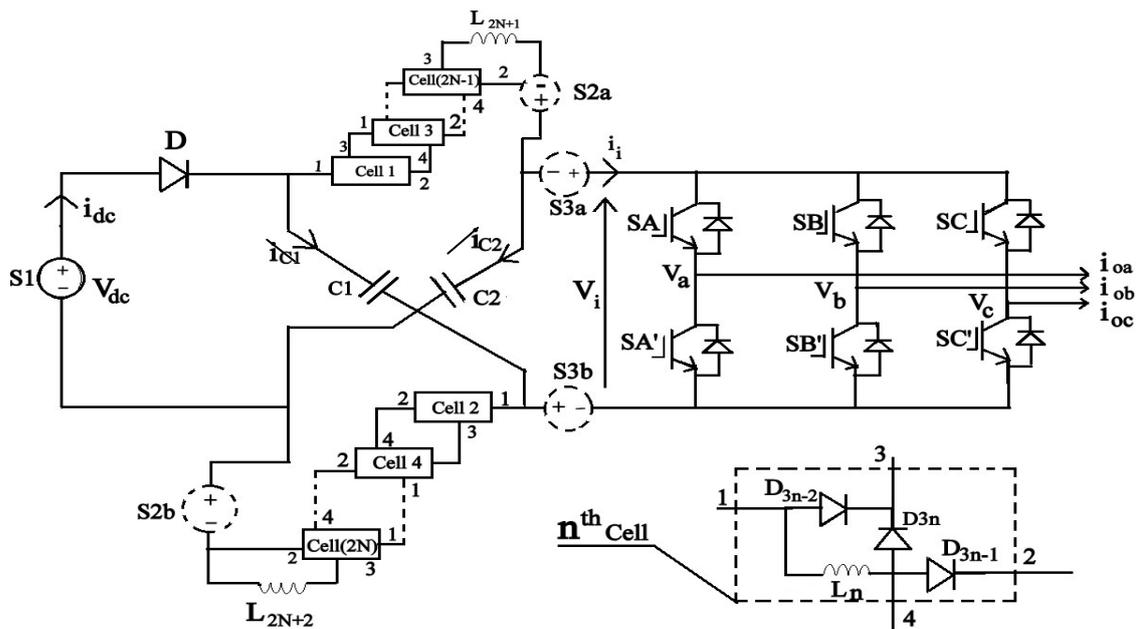


Figure 2. Topology of generalized voltage type SL Z-Source Inverter

These cells must introduce additional inductors in parallel during shoot-through charging and more inductors in series during nonshoot-through discharging. Features and expressions for the two processes are summarized as follows

Shoot-Through: Initiated by turning on two switches from the same phase leg of the VSI bridge. That causes diodes D and D_{3n} to turn OFF, while diodes D_{3n-1} and D_{3n-2} conduct. All inductors are then charged in parallel by the two Z-source capacitors, giving rise to a common inductive voltage of $V_L = V_C$.

Nonshoot-Through: Represented by one of the traditional active or null VSI states. In this state, diodes D and D_{3n} conduct, while diodes D_{3n-1} and D_{3n-2} block. All inductors then discharge in series to the external ac load, whose common inductive voltage is written as $V_L = (V_{dc} - V_C)/(N + 1)$, where $N + 1$ is the number of inductors in the upper or lower cascaded block. Averaging V_L over a switching period to zero then gives the following generic expressions for governing the generalized SL Z-source inverter.

$$V_c = \frac{1 - d_{st} V_{dc}}{1 - (N + 2)d_{st}} \quad (1)$$

$$V_i = \frac{1 + Nd_{st} V_{dc}}{1 - (N + 2)d_{st}} \quad (2)$$

$$V_{ac} = \frac{M[1 + Nd_{st}] V_{dc}}{1 - (N + 2)d_{st}} \quad (3)$$

The boost factor is given by $B = (1 + Nd_{st})/(1 - (N + 2)d_{st})$, which can be made higher than any of the earlier gains by adding more generic cells. The desired gain is also arrived at a reduced shoot-through duration, whose limit is given $d_{st} < 1/(N + 2)$ is derived by setting the denominator of (3) to be greater than zero. That allows a higher modulation ratio to be used since $M \leq 1.15(1 - d_{st})$. Better utilization of the dc-link, lower component stresses, and better spectral performance linked to a high M can, therefore, be achieved. With these characteristics, the generalized SL topology is likely to find applications in renewable or other clean energy industry, where high boosting gain for grid interfacing is usually needed [13]. A probable example is grid-tied photovoltaic (PV) system, whose implementation will usually involve the sensing of \hat{v}_i directly or indirectly through measuring is given by V_c (since $\hat{v}_i = 2V_c - V_{ac}$ during the nonshoot-through state).

The measured \hat{v}_i can then be regulated constant by adjusting M within the upper limit of $1.15(1 - d_{st})$, while reserving d_{st} for tracking the maximum power point of the PV source. This control arrangement is standard for PV systems, meaning that unforeseen complication is unlikely to surface with the generalized SL inverter[14]. With its \hat{v}_i regulated constant, selecting a suitable voltage rating for its semiconductors is thus quite straightforward as long as they have the instantaneous capacity to carry the peak shoot-through current. Other passive component sizing wise can be approached based on the same sizing requirements outlined in [6] for the traditional Z-source inverter.

3. THREE PHASE VOLTAGE SOURCE INVERTER

The circuit diagram for three-phase VSI topology is shown in Figure 3 and the eight valid switch states are given in Table 1. As in single-phase VSIs, the switches of any leg of the inverter (S_1 and S_4 , S_3 and S_6 , or S_5 and S_2) cannot be switched on simultaneously because this would result in a short circuit across the dc link voltage supply. Similarly, in order to avoid undefined states in the VSI, and thus undefined ac output line voltages, the switches of any leg of the inverter cannot be switched off simultaneously as this will result in voltages that will depend upon the respective line current polarity. During the states 7 & 8 (in table 1) the ac current freewheel through either the upper or lower component which produces zero ac line voltages. The remaining states (1 to 6 in Table 1) produce nonzero ac output voltages. The inverter moves from one state to another to generate a required voltage waveform. Thus the resulting ac output line voltages consist of discrete values of voltages that are V_s , 0, and $-V_s$ for the topology shown in Figure 4. The modulating technique is used to ensure the valid states. In this we also explain in various modes.

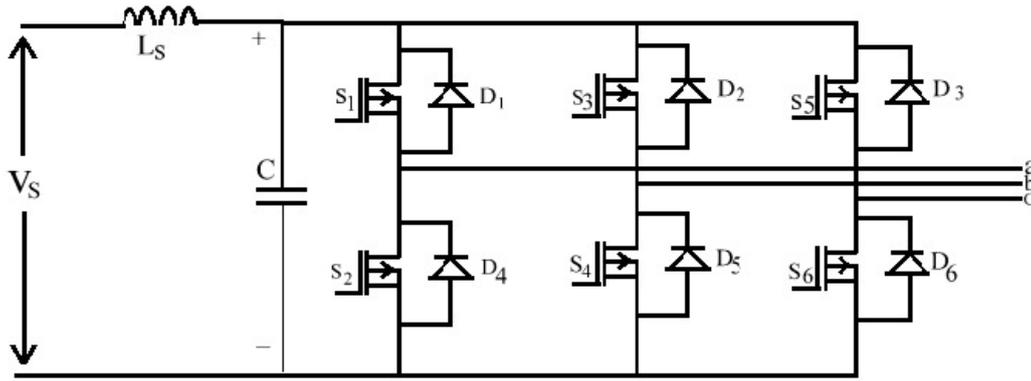


Figure 3. Circuit diagram for Voltage Source Inverter

Table 1. Valid switch states for a three-phase VSI

	State No.	Switch States	V_{ab}	V_{bc}	V_{ca}
S1, S2, S3 on	1	100	V_s	0	$-V_s$
S2, S3, S1 on	2	110	0	V_s	$-V_s$
S3, S4, S2, on	3	010	$-V_s$	V_s	0
S4, S5, S3 on	4	011	$-V_s$	0	V_s
S5, S6, S4 on	5	001	0	$-V_s$	V_s
S6, S1, S5 on	6	101	V_s	$-V_s$	0
S1, S3, S5 on	7	111	0	0	0
S4, S6, S2 on	8	000	0	0	0

The line to neutral voltage must be determined to find the line (or phase) current. There are three modes of operation in a half – cycle and the expression for each mode will be given below,

During Mode I: ($0 \leq t \leq \pi/3$)

$$V_{an} = V_{cn} = \frac{R/2}{R+(\frac{R}{2})} V = \frac{V}{3}, V_{bn} = -\frac{R}{R+(\frac{R}{2})} V = -2V/3 \quad (4)$$

During Mode II: ($\pi/3 \leq t \leq 2\pi/3$)

$$V_{bn} = V_{cn} = -\frac{R}{R+(\frac{R}{2})} V = -\frac{V}{3}, V_{an} = \frac{R}{R+(\frac{R}{2})} V = 2V/3 \quad (5)$$

During Mode III: ($2\pi/3 \leq t \leq \pi$)

$$V_{an} = V_{bn} = \frac{R/2}{R+(\frac{R}{2})} V = \frac{V}{3}, V_{cn} = -\frac{R}{R+(\frac{R}{2})} V = -2V/3 \quad (6)$$

In this consequence, the shape of the modulation index m of the power converter is very similar to the grid voltage waveform. The output voltage of the converter can be written as $V_{out} = mV_{dc}$. Depending on the modulation index value, the power converter will be driven by different PWM strategies. As a matter of fact, it is possible to identify four operating zones (see Figure 3), and for each zone [15], the output voltage levels of the power converter will be different

4. PULSE WIDTH MODULATION

PWM is a very efficient way of providing intermediate amounts of electrical power between fully on and fully off. A simple power switch with a typical power source provides full power only, when switched on. PWM is a comparatively recent technique, made practical by modern electronic power switches [3].

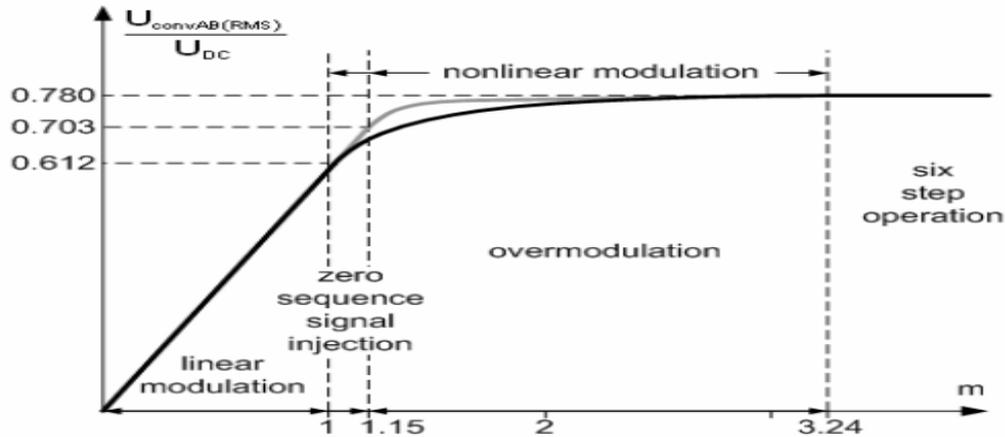


Figure 4. PWM for the DC line side converters

Figure 4 presents the dependence of the converter input voltage on the modulation index with respect to the DC-link voltage. The modulation bandwidth is generally divided into the linear and the nonlinear range. The limitation of the modulation region to the linear range is sufficient for the proper operation of the PWM rectifier. Yet for the excellent dynamic performance of the synchronous rectifier during the transients the operation in the over modulation range must be provided [8]. However this technique introduces the line current distortions due its nonlinearity and may be in advisable in the applications of the DC converters improving the electrical power quality. The issue of the modulation index and the modulation range for the basic PWM techniques will be presented in detail in the next sections of this paper

5. SINUSIODAL PULSE WIDTH MODULATION

There are three sinusoidal reference waves (V_{ra} , V_{rb} , and V_{rc}) each shifted by 120° . A carrier wave is compared with the reference signal corresponding to a phase to generate the gating signals for that phase. Comparing the carrier signal V_{cr} with the reference phases V_{ra} , V_{rb} , and V_{rc} produces S1 and S3 respectively as shown in Figure 5b. The instantaneous line – to – line output voltage is $V_{ab} = V_s(S1 - S3)$. The output voltage as shown in Figure 5d is generated by eliminating the condition that two switching devices in the same arm cannot conduct at the same time. The normalized carrier frequency mf should be odd multiple of three. Thus, all phase – voltage (V_{an} , V_{bn} , and V_{cn}) are identical, but 120° out of phase without even harmonics; moreover, harmonics at frequencies multiple of three are identical in amplitude and phase in all phases. For instance, if the ninth harmonic voltage in phase ‘a’ is

$$V_{an9}(t) = v_9 \sin.9\omega t. \quad (7)$$

The ninth harmonic in phase b_n will be,

$$V_{bn9}(t) = v_9 \sin(9(\omega t - 120^\circ)) \quad (8)$$

$$= v_9 \sin(9\omega t - 1080^\circ) \quad (9)$$

$$= v_9 \sin 9\omega t \quad (10)$$

6. SIMULATION & RESULTS

Comparative analysis is done by using Matlab/Simulink model for PWM and SPWM in terms of THD for Motor load

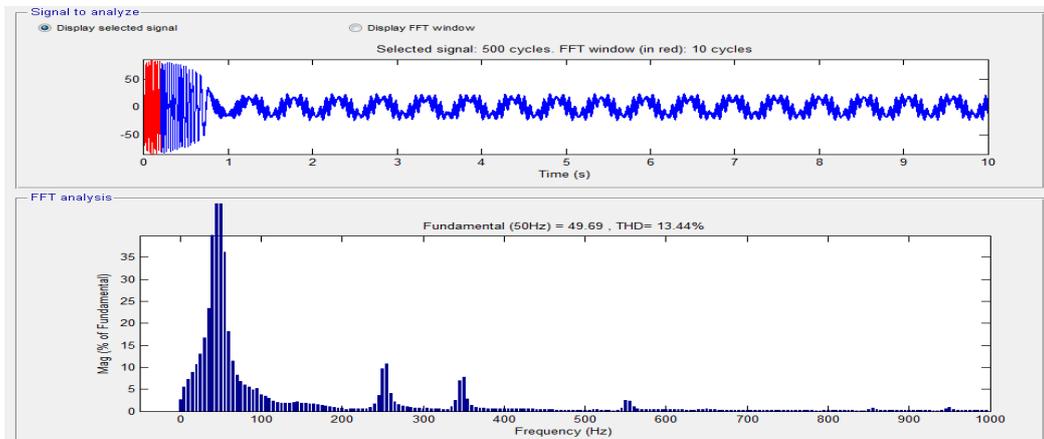


Figure 6. THD for Rotor current with PWM Technique

The simulation results for PWM Technique is determined with THD Analysis for which the rotor current it has 13.44%.

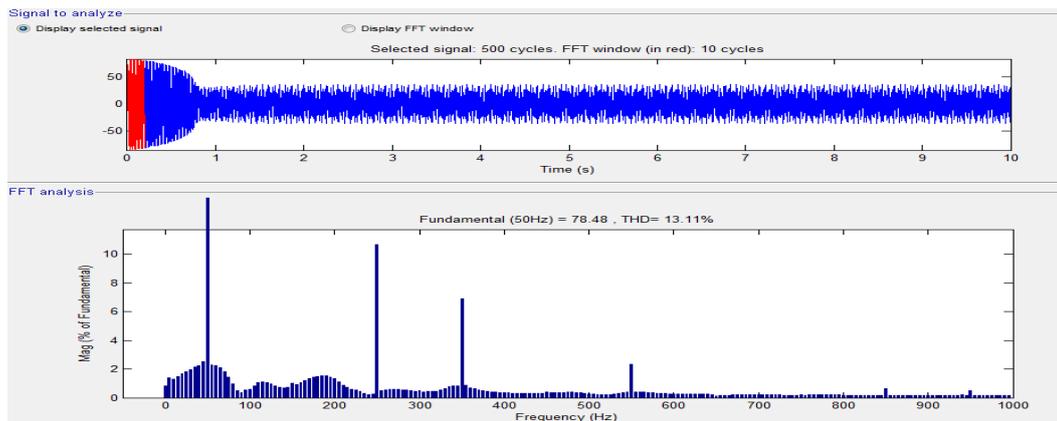


Figure 7. THD for Stator current with PWM Technique

The above simulation results for PWM Technique is determined with THD Analysis for the stator current 13.11%.

Implementation of Sinusoidal PWM technique in the three phase inverter for the induction drive is shown in the Figure 8. The results for the same are shown in the following sections. Both the circuits differ only by the PWM technique used. The harmonics reduction is the major reasons behind using the sinusoidal PWM. The improvement in the performance of the induction motor is thus achieved. Figure 9 shown the rotor current per phase and the harmonic content and in Figure 10 harmonic content in the stator current is analyzed and shown.

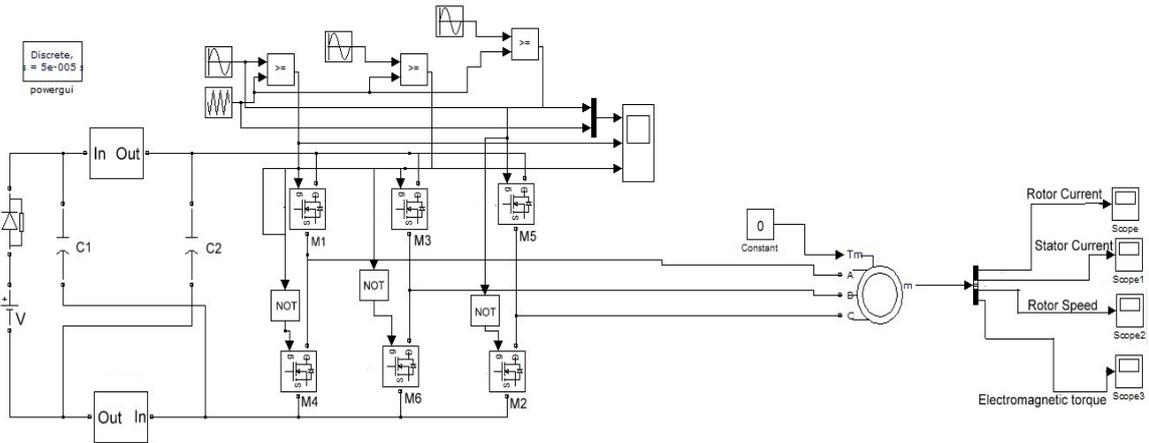


Figure 8. Simulation for Motor load with SPWM Technique

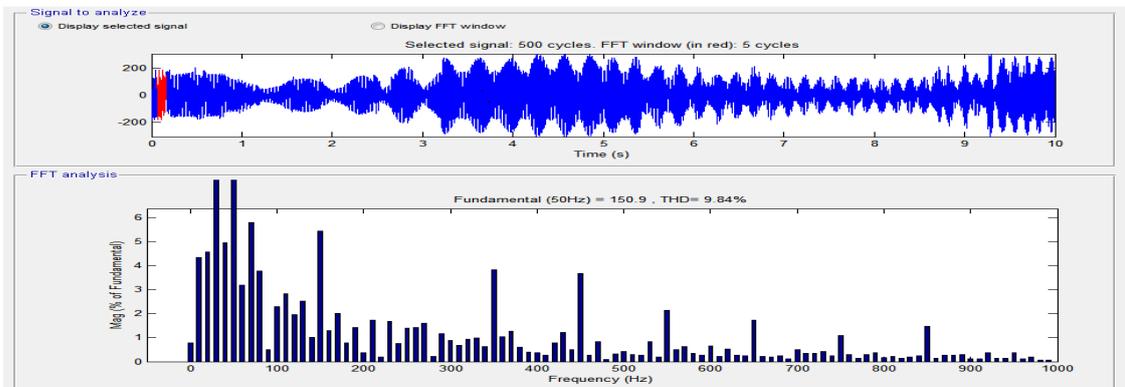


Figure 9. THD for Rotor Current with SPWM Technique

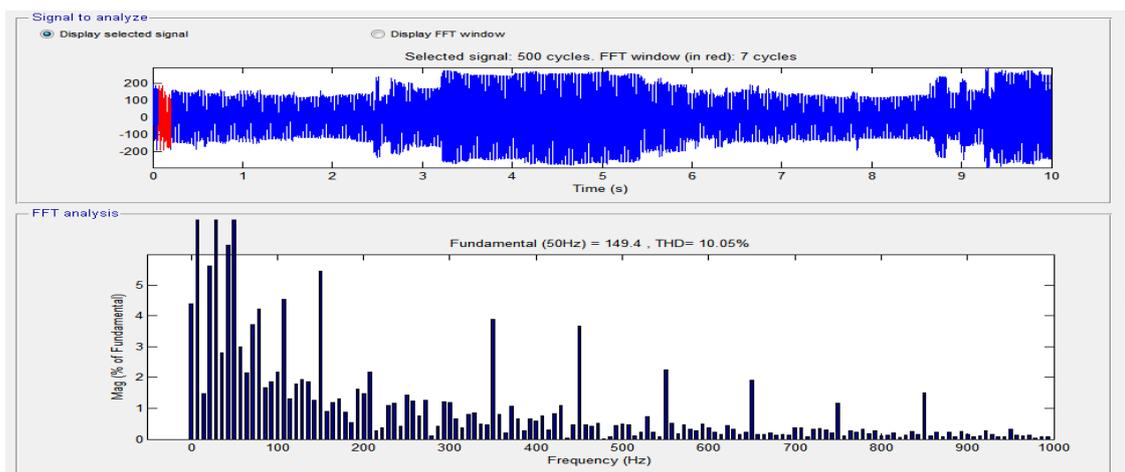


Figure 10. THD for Stator Current with SPWM Technique

The above Simulation results shown for rotor current and stator current, whose rotor current is 9.84% and stator current has 10.05% with Sinusoidal Pulse Width Modulation Technique. The input voltage applied for PWM Technique and SPWM Technique is 440volts.

7. CONCLUSION

This paper has deals with a Multicell with Z-Source inverter solution for Three phase Induction motor. The PWM strategy was chosen in order to obtain the minimum number of commutations to maximize efficiency. The proposed solution was compared with the PWM technique and SPWM technique. By using PWM Harmonics are more. To overcome this disadvantage SPWM technique is used by using this switching losses are controlled and harmonics are reduced compared to PWM method. Finally the PWM and SPWM controlled Multicell Z-Source Inverter is analyzed by Simulation results are obtained and resulting in stability improvement.

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